A NOVEL BPSK DEMODULATOR USING THE EXPECTATION MAXIMIZATION ALGORITHM

Takis Kasparis
Department of Electrical and Computer Engineering
University of Central Florida
Orlando, FL 32816
e-mail: tnk@ece.engr.ucf.edu

Gregory Powell
Koos Technical Services, Inc.
385 Commerce Way, Suite 101
Longwood, FL 32750

ABSTRACT

A novel coherent demodulator is proposed which utilizes the Expectation-Maximization (EM) algorithm for carrier phase recovery. The EM algorithm is feed-forward, and therefore produces no carrier phase error to be fed back to the down conversion process. The algorithm produces a maximum likelihood estimate of the modulating bit sequence, given the received in-phase and quadrature-phase data. Previously, the EM algorithm has been used to demodulate Binary Phase Shift Keying (BPSK) modulated signals, but assumed perfect symbol synchronization. This work combines the EM algorithm with a symbol timing estimation (TE) algorithm to produce a complete BPSK demodulator. The results of the TE algorithm are used to control a polyphase matched filter, which performs root-raised cosine matched filtering as well as symbol timing correction. Simulation results show that the proposed demodulator performs within 1 dB of theory, given constant carrier phase error and/or constant symbol timing error. The demodulator performs within 0.75 dB of theory given a carrier frequency offset of 1.5% of the symbol rate.

I. INTRODUCTION

Digital communications systems have been used for many years to transport information from one user to another. Most frequently, digital communications systems are modeled and designed after analog systems digital filters replace analog filters, numerically controlled oscillators (NCOs) replace voltage controlled oscillators (VCOs), etc. The analysis of these digital communications systems parallels the analysis of their analog counterpart along with the additional complications due to the A/D conversion process such as spectral replication, dynamic range and other factors. More recently, significant research in digital communication systems has focused on new ways to perform the demodulation function that are very different from conventional methods. Usually, the research focuses on one aspect of the demodulation process such as carrier recovery or symbol timing recovery. In this work, a demodulator is examined that combines some of these new techniques to form a complete demodulator that includes carrier recovery and symbol timing recovery. Carrier recovery in conventional coherent BPSK demodulators is frequently accomplished using a Costas loop [5][6]. This loop consists of a symbol phase detector which provides a timing error, a loop filter which smoothes the error values out of the phase detector, and a VCO to provide the sampling frequency to the A/D.

In this work, both the carrier recovery and symbol timing recovery functions are replaced by non-conventional signal processing algorithms. Carrier recovery is accomplished using the Expectation Maximization (EM) algorithm. This method of carrier recovery was introduced in [1] where the EM algorithm for carrier recovery is derived, and an implementation formulated. This algorithm is used in this work with the significant difference that perfect

symbol timing is not assumed. Symbol timing recovery is accomplished using a symbol timing estimator (TE) algorithm introduced in [4]. The algorithm is modified in this work to operate on random data, while the algorithm implemented in [4] assumed a know data sequence in the preamble of a burst communication channel. The TE algorithm will control a polyphase matched filter to perform the symbol phase adjustment.

II. A NOVEL BPSK DEMODULATOR

The focus of this work is a novel coherent BPSK demodulator utilizing the Expectation Maximization (EM) algorithm for carrier recovery, and a symbol Timing Estimation (TE) algorithm. A block diagram of the demodulator is given in Figure 1. The input to the modulator r(t), represents the BPSK signal plus additive white Gaussian noise (AWGN), centered around an IF frequency. The signal is first mixed down to baseband via the quadrature mixer, using the non-coherent complex exponential $e^{j(w_C t+\theta)} = \cos(w_C t + \theta) + j\sin(w_C t + \theta)$. While this reference is non-coherent, it is assumed that it is very close to the desired frequency for bringing the IF signal to baseband. The baseband quadrature data is then sampled and quantized using in-phase and quadrature A/D converters.

The sampling rate for the A/D converters is usually 16 samples per symbol. Therefore, as an example, if the bit rate of the system was 128Kbps, then the sampling rate of the A/D converter would be 2.048MHz. Note that this clock is also non-coherent to the incoming signal. However, it is assumed that the frequency offset of this clock is small. It will be shown later, that the affects of frequency offset can be reduced by decreasing the data block size used in the Expectation Maximization (EM) and Timing Estimation (TE) algorithms. The 16 samples per symbol are then input to the in-phase (I) and quadrature-phase (Q) matched filters. These filters also serve to decimate the sampling rate down to two samples per symbo

l. The samples are then input to the DSP algorithms.

This demodulator incorporates the Expectation Maximization (EM) algorithm to perform carrier recovery. The term carrier recovery is not completely applicable to the EM algorithm approach, since the algorithm need not produce the recovered carrier phase error. In this approach, there is no feedback of the phase error to the front end mixers. The EM algorithm provides an estimate of the modulating sequence, given the I and Q channel data. The TE algorithm uses the estimated modulation sequence generated by the EM algorithm, along with two samples per symbol out of the matched filter. This algorithm, independent of carrier phase error, will produce an estimate of the symbol timing offset, which is used to shift the phase of the digital matched filter. In this way, the symbol timing phase is adjusted, without adjusting the A/D clock.

The advantages of using the EM algorithm combined with the TE algorithm are: 1) the need for VCOs or NCOs is eliminated, 2) since the carrier loop is eliminated as the EM algorithm is feed forward, there is no concern over propagation delay through the loop causing instability concerns, 3) the propagation delay through the symbol timing loop is relatively small, since the timing adjustment occurs in the matched filter, not at the A/D, and 4) reduced design complexity resulting in only a few design parameters that must be varied given system requirements.

The block diagram of Figure 1 also shows a differential decoding block. The purpose of this block is to resolve the two phase ambiguity of the BPSK demodulator. As with conventional BPSK demodulators, there are two stable lock points for carrier recovery - 0^o carrier phase offset and 180^o carrier phase offset. Differentially encoding the data at the modulator, and subsequently differentially decoding the data at the demodulator resolves this phase ambiguity at the expense of a performance degradation of approximately 1dB.

III. THE EM ALGORITHM

The Expectation Maximization (EM) algorithm is a method of performing maximum likelihood estimation. For the purposes of this discussion, the problem at hand is to find the maximum likelihood estimate $\hat{\mathbf{m}}$ which solves the equation

$$\hat{\mathbf{m}} = \arg \max_{\mathbf{m}} f(\mathbf{r}|\mathbf{m}) \qquad (1)$$

where $\mathbf{m}$ is the modulating sequence, and $\hat{\mathbf{m}}$ is an estimate of the modulating sequence. The vector $\mathbf{m}$ is the antipodal waveform consisting of +1's and -1's which represent the binary data 1's and 0's that are sent through the communication system. The vector $\mathbf{r}$ is the received data input to the demodulator. The purpose of a maximum likelihood estimator is to find an estimate of the vector $\mathbf{m}$ which best explains the received data $\mathbf{r}$. The probability density function of $\mathbf{r}$ given $\mathbf{m}$ is called $f(\mathbf{r}/\mathbf{m})$.

The problem of extracting $\mathbf{m}$ from the received data $\mathbf{r}$ is made difficult because there are several unknown

factors in the communications system that affect **r**. Three of these factors are the unknown carrier phase θ, carrier frequency offset o_f, and the unknown sampling error τ. Assuming for the time being that f_o and τ are zero, a set of data which includes **r** and θ (if we had both pieces of information) would make the problem of estimating **m** much easier. The EM algorithm refers to the data (**r**, θ) as "complete data". If a new probability density function is formed f(**r**,θ/**m**), the EM algorithm can be stated as the following 2 step process.

1) Find the expectation of the log likelihood function $f(\mathbf{r},\theta|\hat{\mathbf{m}})$ given **r** and $\hat{\mathbf{m}}^{(i)}$
2) Find $\hat{\mathbf{m}}^{(i+1)}$ that maximizes the expected value found in step 1).

The first step is referred to as the expectation step, and the second step is the maximization step. The two step algorithm is iterated until convergence is achieved. Convergence of the algorithm is based on the point when the expectation value changes less than a pre-determined threshold value from one iteration to the next. A demodulator based on the EM algorithm was demonstrated in [1]. The derivation of the implementation of the algorithm is discussed in [1] and [2]. The complete EM algorithm as given in [1], is summarized the following steps. Let:

1) set i = 0, $m_c^{(0)} = 1$, $m_s^{(0)} = 0$ (no phase offset)
2) find $m^{(i)}$, using the equation

$$\text{if } R_e(r_k)m_c^{(i)} + I_m(r_k)m_s^{(i)} \geq 0, \text{ then } \hat{m}_k = 1 \qquad (2)$$

$$\text{if } R_e(r_k)m_c^{(i)} + I_m(r_k)m_s^{(i)} < 0, \text{ then } \hat{m}_k = -1.$$

3) Compute $m_c^{(i+1)}$ and $m_s^{(i+1)}$, using $m^{(i)}$ and equations

$$m_c^2 = \frac{A_c^2}{A_c^2 + A_s^2} \qquad m_s^2 = \frac{A_s^2}{A_c^2 + A_s^2} \qquad (3)$$

where,

$$A_c = \left[\sum_{k=0}^{N-1} m_k R_e(r_k)\right],$$

$$A_s = \left[\sum_{k=0}^{N-1} m_k I_m(r_k)\right] \qquad (4)$$

4) find $m^{(i+1)}$ using equation (2)

5) If convergence is achieved, output $m^{(i+1)}$, else go to (3)

The algorithm is iterated until the expected value of the log likelihood function changes less than a threshold value, from one iteration to the next.

IV. SYMBOL TIMING ESTIMATION ALGORITHM

Coherent demodulation of BPSK signals requires that the symbol timing be recovered from the received waveform. Before describing the algorithm used in this work for symbol timing recovery, a few definitions are needed. For the digital demodulator of this work, the samples of the received waveform that exit the matched filter occur at two samples per symbol. If it is assumed that the demodulator has acquired symbol timing synchronization, then the two sampling points can be defined as shown in Figure 2. The sample occurring at the peak (maximum energy point) of the symbol is referred to as0the on-time sample. The sample occurring at the symbol transition point is referred to as the off-time sample. T_b is the symbol interval (which in this case is also the bit interval), and SR is the symbol rate. Two samples per symbol provide enough information to the demodulator to derive the timing error.

In this work, the conventional symbol timing methodology has been replaced with a symbol timing estimation (TE) algorithm. The TE algorithm is adopted from [4], where it was used to make an estimate of the symbol timing error during the preamble of a burst communication channel. The estimate was used to provide a one time adjustment of the symbol timing, to bring the sampling to within $\pm 1/8^{th}$ of a symbol from on-time. The algorithm utilizes four pattern correlators to discover where the two samples reside in the symbol interval. In this new application of the TE algorithm, the modulating data sequence **m** is a random binary waveform, unlike [4] where the preamble of the burst signal was alternating +1's and -1's. When there is no bit transition between adjacent bits, there is no new information for the correlators to operate on. Therefore, the algorithm as originally defined in [4] is modified such that bit transitions are detected, and if a transition occurs, the correlator β_i is updated. If no transition occurs between adjacent bits, then the correlator is not updated. As shown in Figure 1, matched filters are present in the I and Q channels of the demodulator. Four functions are performed by these filters. First, since they are matched to the transmitter matched filter, the signal-to-noise ratio (SNR) at the output will be maximized. Second, intersymbol interference (ISI) is reduced since

the filter characteristic is root-raised cosine (RRC) [6]. Third, the receiver matched filters are decimating filters. While the filter operates at 16 samples per symbol, the output of the filter is taken at a rate of twice per symbol. Two samples per symbol are all that is required by the demodulator algorithms. The fourth function of the filters is to shift the phase of the two samples that exit the filters. The phase shift required is commanded by the TE algorithm.

The concept of the digital polyphase filter is to store several sets of filter coefficients in memory, each set representing a different phase of the receiver matched filter. By selecting a different coefficient bank, the phasing of the output samples is changed. The symbol timing estimation (TE) algorithm is used to discover which of the stored filters should be utilized to achieve on-time sampling. The results of the TE algorithm are then used to switch the polyphase matched filter to the proper set of coefficients (or coefficient bank). In this way, the sampling point of the two samples per symbol entering the algorithms is adjusted. Note that the sampling frequency of the A/D converters is not adjusted, thus eliminating the need for a VCO or NCO to adjust the sampling point. The matched filter chosen for this work is root raised cosine (RRC). The polyphase filter in this work consists of four filters, each representing a different constant phase offset. The particular matched filter chosen is based on which of the correlators has the maximum output value at the conclusion of the TE algorithm. The two algorithms discussed in Sections III and IV are combined to form the complete demodulator. As described previously, two samples per symbol are output from the matched filters and presented to the DSP algorithms. The EM algorithm requires only one sample per symbol while the TE algorithm requires two samples per symbol to recover an estimate of the symbol timing error so that the matched filters can be adjusted.

V. SIMULATION RESULTS

This section presents simulation results to show how well the proposed digital demodulator will perform under various scenarios. The demodulator parameters that can be adjusted are the EM algorithm block size N, the TE algorithm correlator length L, and the number of EM blocks per TE algorithm B. Additionally, sources of error are injected into the system including 1) carrier phase offset, 2) carrier frequency offset, 3) symbol timing offset, and 4) various amounts of AWGN . The adjustable demodulator parameters will affect the performance of the demodulator. Qualitatively, the following statements can be made (some quantitative analysis will be given later). The performance of the EM and TE algorithms are independent of a constant carrier phase offset. However, carrier frequency offset is a time varying phase offset - the greater the frequency offset, the faster the phaser in the I-Q plane rotates around the unit circle. The EM and TE algorithms will exhibit degraded performance when the frequency offset becomes large enough so that the carrier phase is not fairly constant for a given block of data input to the algorithms. Therefore, the chosen EM block size N must depend on the carrier frequency offset in the communication system. The same is true for the TE algorithm. In this case, the size of the correlators L must be adjusted to account for frequency offset. This is due to the fact that the TE algorithm receives input from the EM algorithm, but also utilizes the on-time and off-time I and Q samples from the matched filters. The same argument then holds true for the TE and the EM algorithms - performance will be degraded when the carrier phase error cannot be assumed to be constant over the block. Symbol timing offset will also degrade the performance of the demodulator in several ways.

There are several parameters of the demodulator that can be tracked to judge how the algorithms are performing. Because of space limitations only the bit error rate (BER) will be considered. The performance of the demodulator is first studied under ideal conditions, so that it can be shown how varying algorithm parameters will affect performance. After the ideal case is examined, performance will be shown with errors in the system such as carrier phase offset, symbol timing error, and carrier frequency offset.

The first case studied defines the EM block size to be 20. The TE correlator length L=10, and 2 EM blocks (B=2) are used per TE calculation. A typical bit error rate (BER) curve for the demodulator when there is no carrier phase error and no symbol timing error in the system is shown in Figure 3. In this plot, the performance of the demodulator is compared against the theoretical probability of bit error for differentially encoded, coherently detected BPSK communication systems. Figures 4 and 5 present the BER for other signal lengths. Simulated results are represented by the diamonds in the plots. It can be seen from these plots that under these conditions, there is negligible performance degradation.

Now that the proposed demodulator has been studied under ideal conditions, carrier phase error or frequency error, and symbol timing error will be introduced into the system. The BER performance for the case where $\theta = 3\pi/2$ is given in Figure 6. When symbol timing error is introduced into the system, the demodulator is forced to synchronize to the received waveform. This is in

contrast to the previous cases where there was no error in the system, or there was only a constant carrier phase error. Since the demodulator always begins processing assuming that the timing error is zero, the initial choice of the matched filter coefficient set will not be optimal. Therefore, the on-time samples input to the EM algorithm will be degraded, if and until the proper polyphase matched filter index can be found. It will be shown that the demodulator does acquire synchronization, and the proper polyphase matched filter index is discovered. The BER of the demodulator is plotted in Figure 7 for the case where the symbol timing offset is $T_b/2$. This is the most difficult case for the demodulator with regard to acquisition, since the samples given to the EM algorithm initially are off-time samples. Very little accurate information is present in these beginning samples. Similar results to those just presented occur when the timing error is set to $3T_b/4$. The demodulator in this case will acquire and settle on a matched filter. This condition is less difficult, as the timing error is closer to the starting point of the demodulator, which in matched filter index 0. In Figure 8, the symbol timing error is set to $T_b/8$. Under this condition, where the timing offset is exactly between two matched filters, the BER performance suffers. The timing error can not be brought closer than $1/8^{th}$ of a symbol.

Until now, the error sources added to the system have been constant. Now, the effect of a carrier frequency offset will be considered. A frequency offset can be thought of as a phase which changes over time. Under these conditions, as mentioned earlier, it is necessary that the phase be held relatively constant for the duration of the EM block and TE block. Figure 9 shows the BER performance of the proposed demodulator fo = 1/64. The degradation is almost 0.8dB from theory. The effects of the frequency offset can be minimized by reducing the EM block size. When this is done, the frequency offset results in a more constant carrier phase error for the duration of the data blocks.

These simulation results show that the EM block size, and the TE block size, must be adjusted based on the system specifications. The block size should always be chosen such that the phase varies by less that approximately 45^o over the EM block of received bits, to keep the performance within approximately 0.75dB of theory. It must be remembered that there is a tradeoff to be made when the EM block size is reduced. Reducing the EM block size will result in a performance degradation as well. However, the tradeoff is worth making since the degradation due to frequency offset is significantly greater than the degradation due to block size reduction, particularly when the expectation of the log likelihood function is passed from the processing of one EM block to the next.

VI. CONCLUSION

A novel BPSK demodulator using the Expectation Maximization (EM) algorithm for carrier recovery was presented and tested in this work. Utilizing the EM algorithm for carrier recovery in digital communications systems is a fairly recent concept, and the integration of this algorithm along with a symbol tracking algorithm to form a complete demodulator had not previously been done. This implementation of a coherent demodulator requires no VCO's for tracking the carrier and the symbol timing. While the algorithms may be somewhat complex to implement in real time, the number of parameters to adjust based on system requirements is few.

Simulations were used to test the proposed demodulator and indicated that this demodulator will perform within approximately 1dB of theory worst case, assuming no frequency offset. This worst case performance assumes that the symbol timing error is located exactly between the available polyphase matched filters. When the timing error is not at this value, the demodulator performance is much better (within 0.25dB of theory). It was shown that the EM algorithm performs sequence estimation independent of carrier phase (as long as the phase is constant). The TE algorithm was also found to perform independent of a constant carrier phase offset. When frequency offset is added to the system, the demodulator BER performance was within 0.75dB of theory when the EM block size was chosen appropriately.

REFERENCES

[1] J. Qin, "Demodulation Of Binary PSK Signals Without Explicit Carrier Synchronization," *Proceedings of the 1993 IEEE International Conference on Communications*, 1993, pp. 498-501.

[2] G. M. Powell, "A Demodulator for Binary Phase Shift Keying Using EM Carrier Recovery and Polyphase Filtering," Masters Thesis, The University of Central Florida, 1996.

[3] C. N. Georghiades, and D. L. Snyder, "The Expectation-Maximization Algorithm for Symbol Unsynchronized Sequence Detection," *IEEE Trans. on Communications*, vol. 39, No. 1, January 1991, pp. 54-61.

[4] C. Heegard, J. A. Heller, and A. J. Viterbi, "A Microprocessor-Based PSK Modem for Packet

Transmission Over Satellite Channels," *IEEE Trans. on Communications*, vol. COM-26, No. 5, May 1978, pp. 552-564.

[5] L-N. Lee, A. Shenoy, and M. K. Eng, "Digital Signal Processor-Based programmable BPSK/QPSK/offset-QPSK Modems," *COMSAT Technical Review*, vol. 19, No. 2, Fall 1989, pp. 196-233.

[6] B. Sklar, *Digital Communications Fundamentals and Applications*, P T R Prentice-Hall, Inc., ISBN 0-13-211939-0 025, 1988.

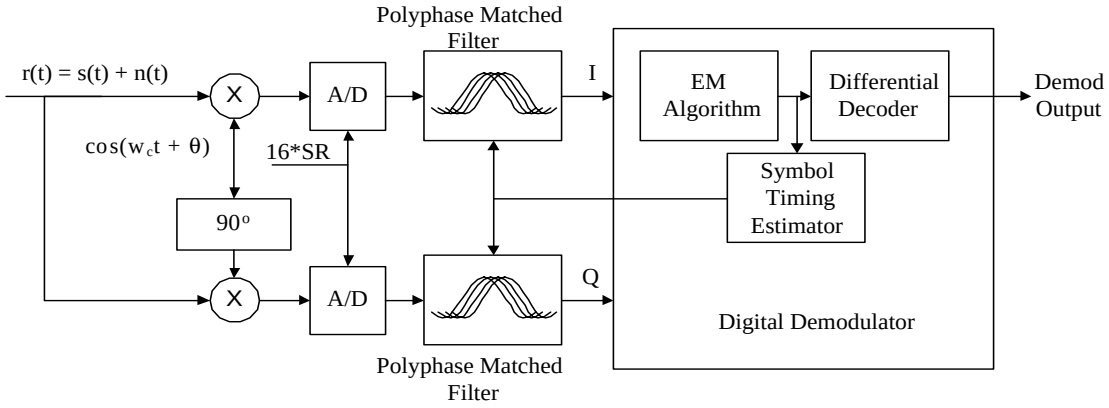

Figure 1. Novel BPSK Demodulator

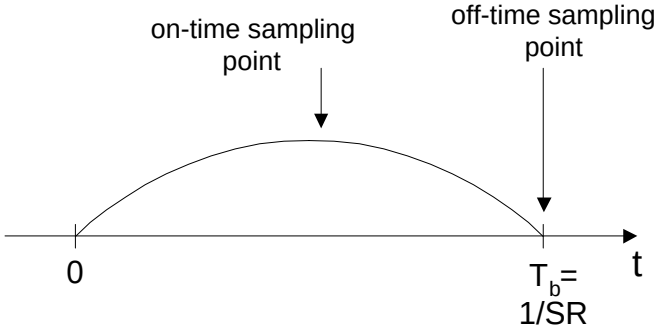

Figure 2. Symbol Timing for 2 Samples per Symbol

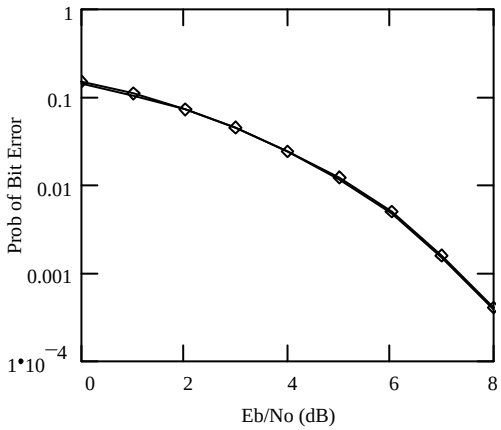

Figure 3. Pb, EM Block Size=20, TE L=10, TE B=2, No Phase Error, No Timing Error

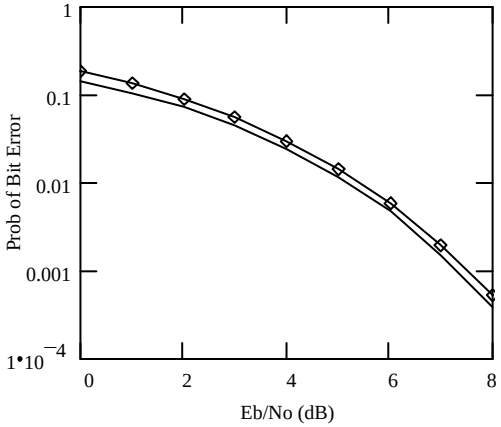

Figure 4. Pb, EM Block Size=5, TE L=10, TE B=4, No Phase Error, No Timing Error

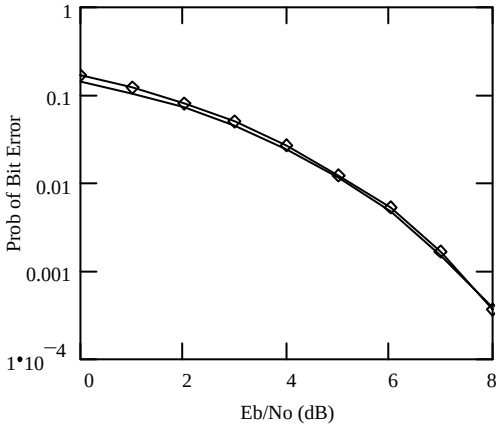

Figure 5. Pb, EM Block Size=5, TE L=10, TE B=8, No Phase Error, No Timing Error

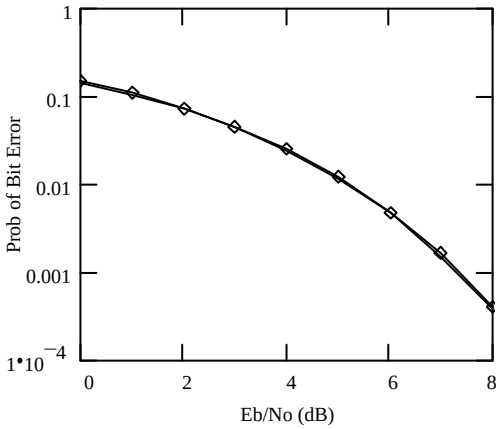

Figure 6. Pb, EM Block Size=20, TE L=10, TE B=2, Phase Error=3π/2, No Timing Error

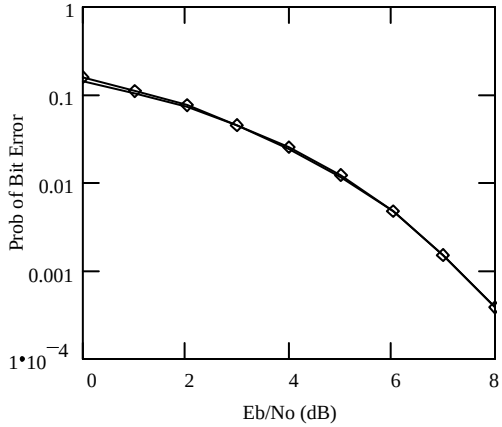

Figure 7. Pb, EM Block Size=20, TE L=10, TE B=2 No Phase Error, Timing Error=$T_b/2$

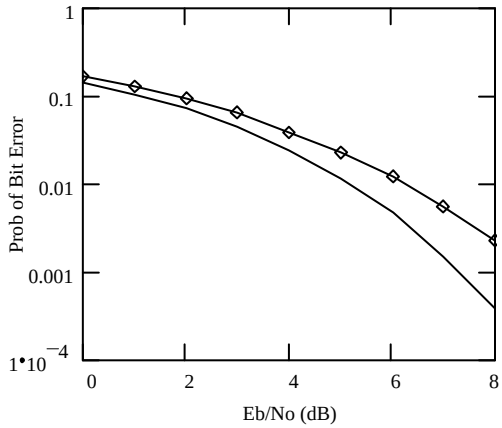

Figure 8. Pb, EM Block Size=20, TE L=10, TE B=2, No Phase Error, Tim ing Error=$T_b/8$

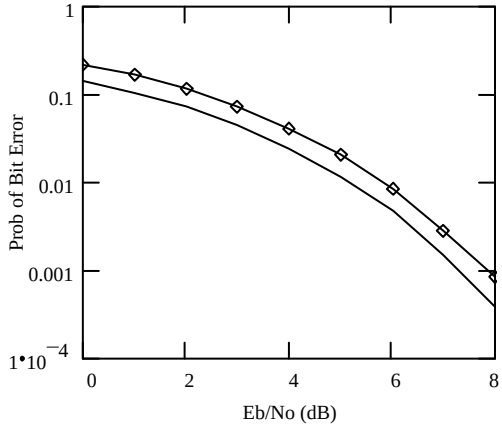

Figure 9. Pb, EM Block Size=5, TE L=10, TE B=8, f_o=1/64, No Timing Error